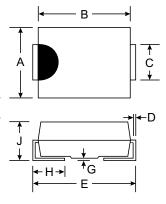


3.0A SURFACE MOUNT SUPER-FAST RECTIFIER

Features

- Glass Passivated Die Construction
- Super-Fast Recovery Time For High Efficiency
- Low Forward Voltage Drop and High Current Capability
- Surge Overload Rating to 100A Peak
- Ideally Suited for Automated Assembly
- Plastic Material: UL Flammability Classification Rating 94V-0



	SMC					
Dim	Min	Max				
Α	5.59	6.22				
В	6.60	7.11				
С	2.75	3.18				
D	0.15	0.31				
E	7.75	8.13				
G	0.10	0.20				
Н	0.76	1.52				
J	2.00	2.62				
All Dimensions in mm						

Mechanical Data

Case: Molded Plastic

- Terminals: Solder Plated Terminal Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band or Cathode Notch
- Weight: 0.21 grams (approx.)
- Mounting Position: Any
- Marking: Type Number

Maximum Ratings and Electrical Characteristics @ TA = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

Characteristic		Symbol	US3A	US3B	US3C	US3D	US3F	US3G	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage		V _{RRM} V _{RWM} V _R	50	100	150	200	300	400	V
RMS Reverse Voltage		V _{R(RMS)}	35	70	105	140	210	280	٧
Average Rectified Output Current	@ T _A = 55°C	lo	3.0					Α	
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave Superimposed on Rated Load (JEDEC Method)		I _{FSM}	100						А
Forward Voltage	@ I _F = 3.0A	V _{FM}	0.95 1.25				25	٧	
Peak Reverse Current at Rated DC Blocking Voltage	@ T _A = 25°C @ T _A = 150°C	I _{RM}	5.0 50				μА		
Reverse Recovery Time (Note 3)		t _{rr}	35						ns
Typical Junction Capacitance (Note 2)		Cj		5	0		3	0	pF
Typical Thermal Resistance, Junction to Terminal (Note 1)		R ₀ JT	15						K/W
Operating and Storage Temperature Range		T _j , T _{STG}	-65 to +150					°C	

Notes

- 1. Unit mounted on PC board with 5.0 mm² (0.013 mm thick) copper pads as heat sink.
- 2. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.
- 3. Measured with $I_F = 0.5A$, $I_R = 1.0A$, $I_{rr} = 0.25A$. See Figure 5.

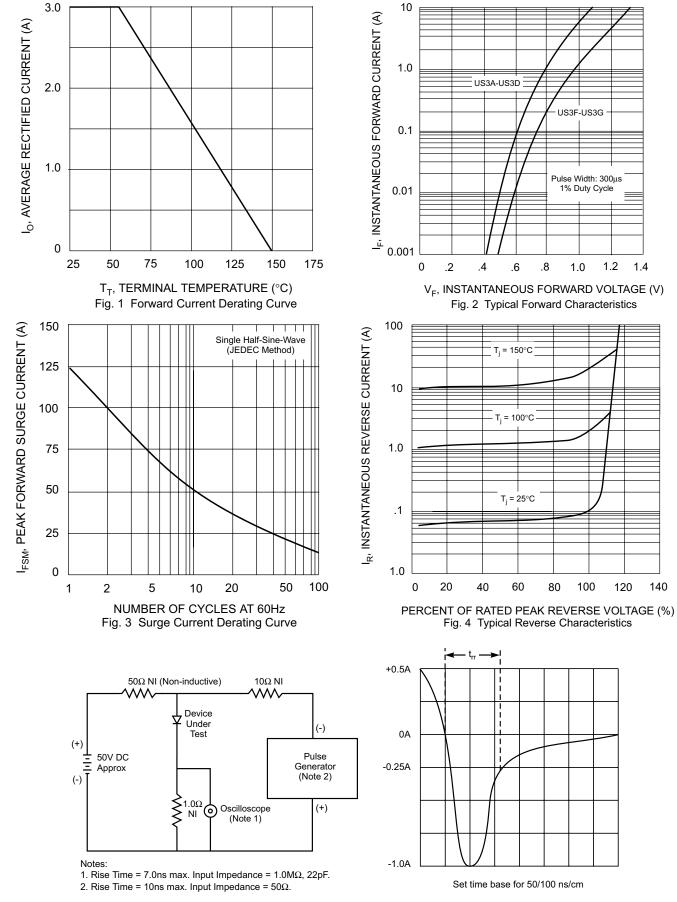


Fig. 5 Reverse Recovery Time Characteristic and Test Circuit